AMENDMENTS TO THE CLAIMS

1. (currently amended) A dual port SRAM cell comprising six nMOS devices,

two nMOS pull-down devices,

two nMOS first pair of transfer devices,

two nMOS second pair of transfer devices,

a first pair of bitlines coupled to the drains of the first pair of transfer devices,

a second pair of bitlines coupled to the drains of the second pair of transfer devices,

a first wordline coupled to the gates of the first pair of transfer devices, and a second wordline coupled to the gates of the second pair of transfer devices,

wherein, when one pair of nMOS transfer devices is activated by its coupled wordline, the other pair of nMOS transfer devices function as load pull-up devices.

2.-3. (cancelled)

4. (original) The dual port SRAM cell of claim 1, wherein said first wordline is the first port for read and write operations.

5. (original) The dual port SRAM cell of claim 1, wherein said second wordline is the second port for read and write operations.

6. (currently amended) A dual port SRAM cell comprising four nMOS and three pMOS devices,

first and second ~~two~~ nMOS pull-down devices,

first and second ~~two~~ pMOS pull-~~down~~ up devices,

first and second ~~two~~ nMOS ~~first pair of~~ transfer devices,

a single ~~one~~ pMOS ~~second~~ transfer device,

first and second ~~a first pair of~~ bitlines coupled respectively to the drains of the first and second nMOS ~~pair of~~ transfer devices,

a third ~~second~~ bitline coupled to the drain of the single pMOS ~~second~~ transfer device,

a first wordline coupled to the gates of the first and second nMOS ~~pair of~~ transfer devices, and

a second wordline coupled to the gate of the single pMOS ~~second~~ transfer device.

7. (original) The dual port SRAM cell of claim 6, wherein said first wordline is the first port for read and write operations.

8. (original) The dual port SRAM cell of claim 6, wherein said second wordline is the second port for read-only operations.

9.-12. (cancelled)

13. (new) The dual port SRAM cell of claim 6, wherein the dual port SRAM cell is composed of only three bitlines.

14. (new) The dual port SRAM cell of claim 6, wherein the dual port SRAM cell is composed of only three transfer devices.